Getting Started Guide

Serial Dual-Port Memory Interface with netX

Hilscher Gesellschaft für Systemautomation mbH

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1 Introduction

1.1 About this Document

This manual guides through the process of interfacing any SPI capable host CPU to a netX-based hardware via the serial dual-port memory (DPM) interface.

1.2 List of revisions

Rev	Date	Name	Chapter	Revision
6	2018-10-04	HHE	All	Description for netX 10 added. Used with COMX 10, NRP 10, etc.

Table 1: List of revisions

1.3 Overview

This manual describes the serial DPM interface of the netX with the aim to support and lead you during the process of interfacing any CPU with a SPI unit, running under your own operating system. The concept of the serial DPM interface is shown in the following figure.

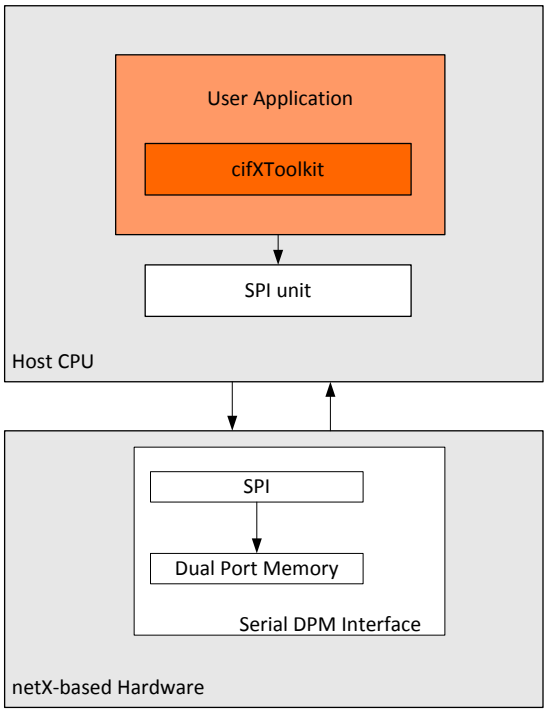

Figure 1: Serial DPM - Architecture

1.4 Requirements

- netX with serial DPM support (see section *Supported hardware* on page 4)
- Host CPU with SPI unit capable to use default SPI Master mode 3 (clock idle state high with sampling on the trailing clock edge), the SPI Clock rate must not exceed 50 MHz for netX 10, netX 51, and netX 52,
- cifXToolkit V1.1.0.0 or higher
- netX Tag List Editor for patching the generic netX 10/51/52 2nd Stage Bootloader.
- Knowledge of the serial DPM protocol (section *Serial DPM Protocol description* on page 10).
- Guideline to port the cifX Toolkit to a custom CPU/OS. See manual [3].

Note: Theoretical up to 125 MHz should be possible (netX 10 / netX 51 / netX 52). Due to existing SPI Controllers max. 50 MHz are verified by tests

1.5 Supported hardware and limitations

The serial DPM is available for netX 10, netX 51, and netX 52.

Overview netX chip serial DPM features

Property	netX 10	netX 51/52
Implementation	Hardware	Hardware
SPI activation	via 2nd stage bootloader	via 2nd stage bootloader
Supported SPI modes	0-3 (default 3) Adjustable via 2nd stage bootloader	0-3 (default 3) Adjustable via 2nd stage bootloader
Maximum SPI clock	125 MHz (until 50MHz confirmed with test runs)	125 MHz (until 50MHz confirmed with test runs)
Address alignment	Byte	Byte

Table 2: Overview netX chip serial DPM feature

1.6 Terms, abbreviations and definitions

Term	Description
ARM	Advanced RISC Machines
CPU	Central Processing Unit
DPM	Dual Port Memory
LSB	Least Significant Bit
MSB	Most Significant Bit
SPI	Serial Peripheral Interface

Table 3: Terms, abbreviations and definitions

1.7 References to documents

This document refers to the following documents:

[1] Hilscher Gesellschaft für Systemautomation mbH: Technical Reference Guide, netX 10, Revision 0.9, English, 2012.

[2] Hilscher Gesellschaft für Systemautomation mbH: Technical Reference Guide, netX 51/52, Revision 3, English, 2017.

[3] Hilscher Gesellschaft für Systemautomation mbH: Toolkit Manual, cifX/netX Toolkit, DPM, V1.5, Revision 10, English, 2018.

Table 4: References to documents

2 Hardware connection

The netX offers an SPI Slave interface which will be used for serial access to the DPM of the hardware. The general connection of the netX serial DPM to any SPI capable host CPU is shown below.

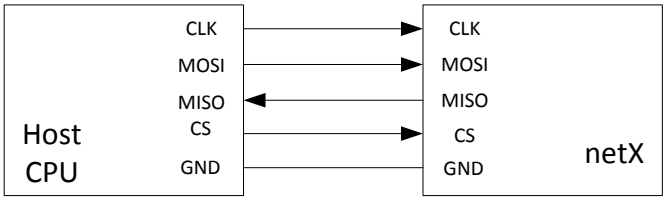

Figure 2: Serial DPM - Hardware Connection

2.1 Pin Connection of netX 10

Please connect the SPI signals of your host CPU to the netX 10 hardware according to the pin connection table.

Function	Pin	netX10 Signal Name
CLK	E14	DPM_D11 / DPM_SPI_CLK
MOSI	G14	DPM_D09/ DPM_SPI_MOSI
MISO	H14	DPM_D08 / DPM_SPI_MISO
CS	F14	DPM_D10 / DPM_SPI_CSn

Table 5: Pin Connection of the netX 10

2.2 Pin connection of netX 51/52

Connect the SPI signals of your host CPU to the netX 51/52 hardware according to the following pin connection table.

Function	netX 51 Pin / Signal Name	netX 52 Pin / Signal Name
CLK	G16 / DPM_SPI_CLK	D18 / DPM_SPI_CLK
MOSI	H15 / DPM_SPI_MOSI	G16 / DPM_SPI_MOSI
MISO	J16 / DPM_SPI_MISO	G18 / DPM_SPI_MISO
CS	H16 / DPM_SPI_CSn	F17 / DPM_SPI_CSn

Table 6: Pin connection of the netX 51/52

3 Enable the serial DPM Interface on the netX

The serial DPM interface is disabled by default. Depending on the netX chip the required action to enable the serial DPM differs. The necessary actions for each netX chip are described in the sections below.

3.1 netX 10/51/52

Activating the serial DPM on netX 10/51/52 is done by the 2nd stage bootloader.

With release of the generic 2nd stage bootloader V1.4.8.0 (V1.4.9.0 for netX51/52 based devices) enabling of serial or parallel DPM is done according to the DIRQ/SIRQ pins. Detailed information about the automatic detection via DIRQ/SIRQ pins is given in the table below.

DIRQ	SIRQ	Mode
0	X	Serial DPM (SPI mode 3)
1	0	16-bit parallel DPM
1	1	8-bit parallel DPM

Table 7: Serial DPM auto detection via DIRQ/SIRQ pin

Function	netX 10 Pin / Signal Name	netX 51 Pin / Signal Name	netX 52 Pin / Signal Name
DIRQ	G12 / DPM_DIRQ	C17 / DPM_DIRQn	D16 / DPM_DIRQn
SIRQ	A12 / DPM_SIRQ	B11 / DPM_SIRQn	C08 / DPM_SIRQn

Table 8: DIRQ/SIRQ pin Connection of the netX 10/51/52

Note: Serial DPM enabled via DIRQ/SIRQ will always work in SPI mode 3. To use a different mode, please consider manual activation of the serial DPM via Tag List Editor.

Furthermore serial DPM access can be enabled explicitly. This can be done by patching the 2nd stage bootloader with the netX Tag List Editor (please note that patching the 2nd stage bootloader will override the auto detection mechanism stated above).

Changing the 2nd Stage Loader DPM handling to SPI

- **For netX 10:** Start the Tag List Editor and load the generic 2nd stage bootloader for netX 10. Change the netX 10 HIF/DPM configuration as shown in the figure below:

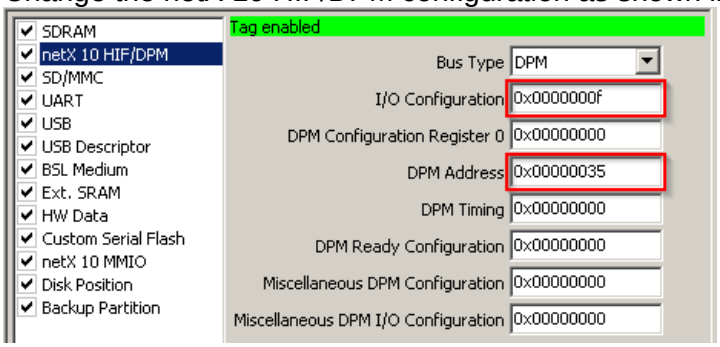

Figure 3: Patching the 2nd Stage Bootloader to enable serial DPM for netX 10

- **For netX 51/52:** Start the Tag List Editor and load the generic 2nd stage bootloader for netX 51/52. Change the netX 51/52 HIF/DPM configuration as shown in the figure below:

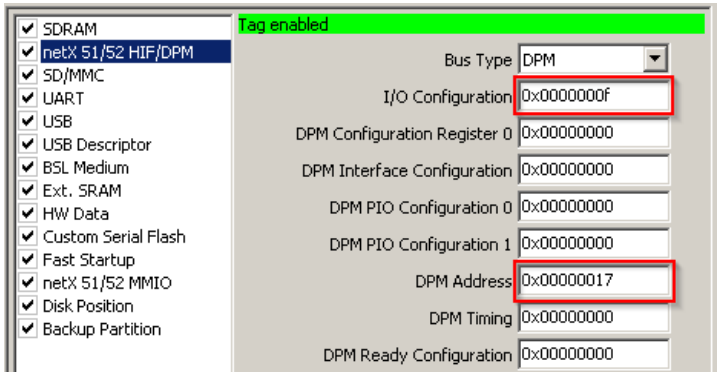

Figure 4: Patching the 2nd Stage Bootloader to enable serial DPM for netX 51/52

Note: To get started, a ready to use 2nd stage bootloader, with activated serial DPM access, is included in the examples.

If you want to use a different SPI mode than the default (mode 3), please consider the table below:

SPI mode	I/O Configuration (see Tag List Editor)
0	0x00000003
1	0x00000007
2	0x0000000B
3 (default)	0x0000000F

Table 9: SPI Mode Configuration (netX 10/51/52)

- Save the changes and flash the 2nd stage bootloader to your netX 10 respectively for your netX 51/52 device

Any netX 10/51/52 compatible fieldbus firmware will now work with serial DPM access.

4 Host software implementation

A Host application will use the CIFX API, offered by all HILSCHER drivers. Basis of the Hilscher drivers is the cifX Toolkit offering the basic access functions to the Hilscher defined DPM.

In general the cifX-Toolkit is independent of any operating system and can be used with or without an operating system and it is scalable.

A short instruction on how to port the cifX Toolkit to your own embedded system is given in reference [3] (section 2: How to port the cifX Toolkit).

To allow the Toolkit to handle netX-based devices which are connected via a SPI interface, an optional custom hardware interface was introduced with release of version 1.1.0.0. This custom hardware interface extends the basic access functions by Read/Write function calls, replacing the default *memcopy()* and pointer access commands used in the Toolkit to access the physical DPM of the netX.

Please refer to the Toolkit Manual [3] (section 4.10: Custom Hardware Access Interface) to get detailed information about the custom hardware interface.

The functional principle of the custom SPI hardware interface is shown on the basis of the *xChannelGetMBXState()* call (see figure below):

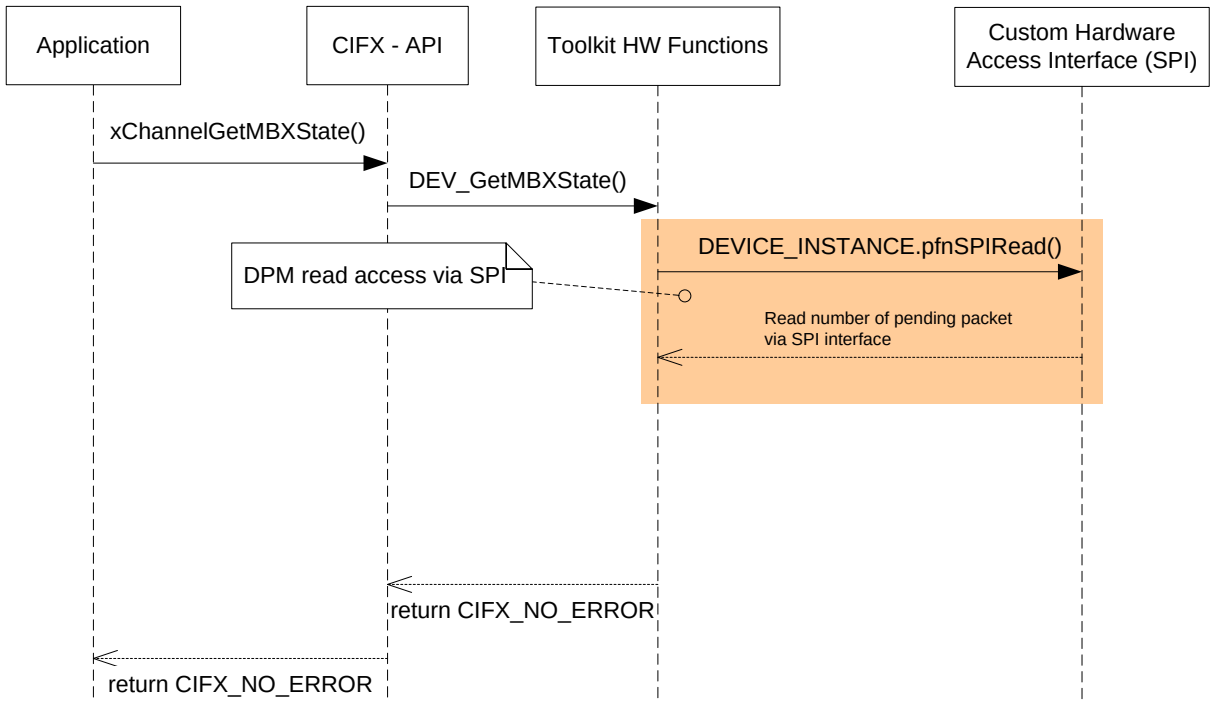

Figure 5: cifXToolkit - SPI Access Interface

The *Read/Write* function calls, to access the SPI unit, must be implemented by the user, since SPI handling depends highly on the used host CPU and host controller. The protocol for accessing the serial DPM differs slightly depending on the used netX chip.

For an easy start refer to the host examples offered with this manual.

5 Serial DPM Protocol description

The general structure of the serial DPM protocol consists of a header and a subsequent data section. The header is always generated by the host CPU SPI Master interfaces via MOSI. It contains address information, control information and length of transfer information.

5.1 netX chip detection

The protocol type can be detected by evaluating the data returned by the netX while transferring the header section of each data transfer.

- netX 10: Returns always 0x00 during transfer of the header section
- netX 51/52 returns: During transfer of the header section first byte returned is the serial DPM status (Status is fine for Bit[0:4] == 0x11)

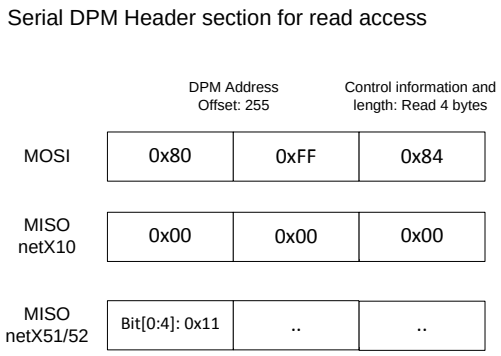

Figure 6: Detect serial DPM protocol

Note: To get started, it is highly recommended to use the examples enclosed with this manual.

5.2 netX10 serial DPM Protocol

Since the serial DPM mode allows direct access to the DPM memory area without any software interaction on netX side (e.g. moving data to and from Send and Receive FIFOs), an access protocol had to be defined which is described below.

The MSB is always transferred first in the serial data. Each transfer starts with a transfer-header and is followed by at least one data byte to be exchanged between host CPU and netX. Transfer header length is 3-byte or 4-byte depending on programmed external address range: less and equal than 64K: 3-Byte, 128K: 4-Byte.

Important: The host has to do **two** read commands to initialize the serial dual-port memory communication (SPI). Any address can be used.

The chip select signal (DPM_SPI_CSn) is used by the DPM interface as asynchronous reset of receive and transmit logic, hence DPM_SPI_CSn must remain active throughout the complete transfer and must become inactive between sequential transfers.

Serial transfers are mapped inside netX DPM interface to standard 8-bit parallel DPM accesses. Hence each transfer must provide the address to be accessed and the access type (read or write) as transfer-header information. Even using small external address range, this information takes at least 3 bytes. To avoid a huge transfer overhead by transmitting the header before each single data byte, the header is followed by a data byte stream. With each data byte, the related address is automatically incremented by one.

Using external address range (DPM size) of 128K requires 4-byte instead of 3-byte header. Header size is derived form the value programmed in external address range configuration register. The default after reset is the smallest supported external address range. Hence after netX 10 reset always 3-byte header must be used. If external address range is configured to 128K, all headers after configuration access to external address range configuration register must be 4-byte headers.

The following table shows the transfer header structure depending on the programmed external address range:

Address range	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
64K or less	Addr. [MSB..8]	Addr. [7..0]	nW/R, length	Data 0	(Data 1)
128K	Addr. [MSB..16]	Addr. [15..8]	Addr. [7..0]	nW/R, length	Data 0

Figure 7: SPI Frame Format (netX 10)

The header is always generated by host CPU SPI interface. First 2 bytes (3 for external address range of 128K) contains address information (MSB first). These bytes are always followed by a control byte. Control byte MSB defines data transfer direction. If this bit is set, the current transfer reads data from netX, otherwise data is written to the netX. The lower 7 bits of the control byte contain transfer length information (number of bytes to be read).

Read accesses through the serial DPM interface, internally always result in read ahead accesses, as otherwise it would not be possible to deliver serial read data on SPI_MISO without data polling or some kind of ready handshake mechanism. To avoid problems with access sensitive address areas (e.g. FIFOs), the number of bytes to be read can be specified in the header, allowing to stop the read-ahead before reaching an access sensitive area. If the transfer length is set to 0, internal consecutive read accesses are done until the transfer is ended by the host by setting SPI_CSn to high level, while there will be always one internal read access beyond the last byte that was actually transferred. The length parameter is ignored for write accesses, as the number of bytes to be written simply arises from the number of bytes transferred by the host before ending the transfer. Please refer to reference [1] (Section 2.9.3 Serial (SPI) DPM interface mode) for detailed information about the serial DPM protocol of the netX 10.

5.3 netX 51/52 serial DPM Protocol

For netX 51/52, basically all serial DPM transfers of SDP2 consist of a header followed by a byte-orientated address-incrementing data stream. All bytes (header and data) are serial transmitted MSB first (i.e. standard SPI). Chip-select signal must remain active all time during an access sequence (inactive chip-select will terminate a transfer). The transfer-header consists always of a direction-bit (read/not-write bit), three command (cmd) bits and a 20 bit address.

Important: The host has to do **two** read commands to initialize the serial dual-port memory communication (SPI). Any address can be used.

To enable straight data stream mode all command bits must be zero. Other settings for command are reserved. The transfer length for read and write access are given in the table below. All headers of a read-sequence are extended by an additional length-byte before the first data byte. This is necessary to avoid problems with read-sensitive addresses (e.g. FIFOs) as read accesses must be performed as read-ahead internally. When a read sequence is not terminated after <length> bytes, invalid read data will be returned. No read access will be done netX inside then.

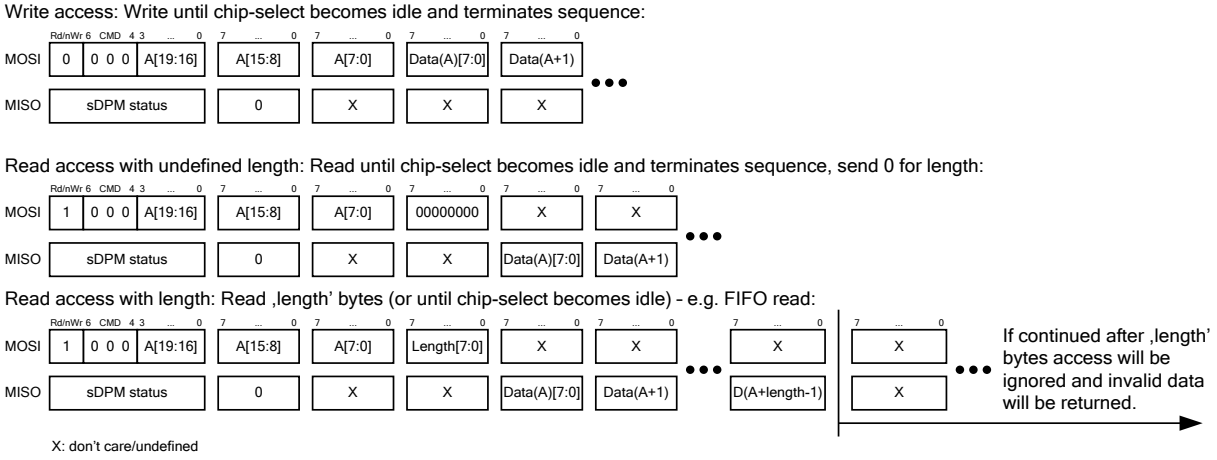

Figure 8: SPI Frame Format for Read/Write Request (netX 51/52)

During the first byte of the header the current serial DPM status will always be clocked out on MISO. This provides information about the current DPM error states and could be used when access timing is unpredictable. See table below.

Bits	Name	Description
7:5	-	reserved (for DPM-SPI read data will be unpredictable)
4	SEL_DPM_SERIAL	DPM_MODE configuration input state. 0: DPM is in parallel mode (DPM_MODE configuration input is low). 1: DPM is in serial mode (DPM_MODE configuration input is high).
3	RDY_TO_ERR	DPM_RDY Timeout Error Status Flag. This error could occur if host device tries to access permanently busy netX address area (e.g. netX xPEC program RAM while xPEC is running). To avoid host device stalling DPM_RDY sig. is released to ready state after 2048 system clock cycles (i.e. 20.48us) at least. 1: Last access went to netX busy address and was broken to avoid host device stalling. 0: Access was finished successfully by DPM_RDY assertion to ready state.
2	WR_ERR	DPM Write Error Status Flag. Write errors occur if ready signal (DPM_RDY) is not respected by host device and external DPM write access terminated before data could be stored. In some cases certain netX address areas could be busy for not predictable time. If DPM_RDY is not used, check for write error after write access to these areas. In case of write error this bit is set immediately after the appropriate write access. Repeat the write access until no error occurs. 1: The external DPM write access was too fast to store write data. Repeat the write access. 0: Write access terminated without error.
1	RD_ERR	DPM Read Error Status Flag. Read errors occur if ready signal (DPM_RDY) is not respected by host device and external DPM read access terminated before read data could be asserted on the external DPM data bus (view also t_rds in dpm_timing_cfg register). In case of read error this bit is set immediately after the appropriate read access. Repeat the read access until no error occurs. 1: The external DPM read access was too fast. Repeat the read access. 0: Read data OK.
0	UNLOCKED	DPM is locked during netX power up and boot phase. DPM access to other addresses than these DPM control address area cannot be done before this bit is set to 1. Poll for 1 after power up or reset.

Table 10: Serial DPM status (netX 51/52)

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6.3 Legal Notes

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